

AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims will replace all prior versions, and listings, of claims in the application:

Please cancel claim 2 and 10 without prejudice or disclaimer.

1. (Currently Amended) A monotonic counter formed as an integrated circuit, each counting bit being provided by a memory cell containing at least one storage element formed of a polysilicon resistor, programmable by irreversible decrease in its value;

wherein the programming of said resistor is performed by temporarily submitting it to a constraint current greater than a current for which its value exhibits a maximum.

2. (Canceled)

3. (Previously Presented) The monotonic counter of claim 1, comprising a circuit for decoding the states contained in said cells for providing the resulting count.

4. (Currently Amended) The monotonic counter of claim 1, wherein each counting cell comprises, in parallel between two terminals[[-]]of application of a supply voltage, two branches each comprising:

a first polysilicon programming resistor connected between a first supply terminal and a terminal of differential reading of the cell state; and

at least one programming switch connecting one of said read terminals to the second supply terminal.

5. (Previously Presented) The monotonic counter of claim 4, wherein each branch comprises a programming switch.

6. (Previously Presented) The monotonic counter of claim 4, wherein said programming resistors are two polysilicon resistors identical in size and in possible doping.

7. (Previously Presented) The monotonic counter of claim 1, wherein each counting cell comprises a programming transistor in series with a programming resistor.

8. (Previously Presented) The monotonic counter of claim 1, further comprising a circuit for controlling the programming of each of the counting cells, capable of providing individual control signals to the programming switches.

9. (Currently Amended) A monotonic counter wherein each counting bit is provided by a memory cell containing at least one storage element comprising a polysilicon resistor, programmable by decreasing its value;

wherein the programming of said resistor is performed by temporarily submitting it to a constraint current greater than a current for which its value exhibits a maximum.

10. (Canceled)

11. (Previously Presented) The monotonic counter of claim 9, comprising a circuit for decoding the states contained in said cells for providing the resulting count.

12. (Previously Presented) The monotonic counter of claim 9, wherein each counting cell comprises, in parallel between two terminals of application of a supply voltage, two branches each comprising:

a first polysilicon programming resistor connected between a first supply terminal and a terminal of differential reading of the cell state; and

at least one programming switch connecting one of said read terminals to the second supply terminal.

13. (Previously Presented) The monotonic counter of claim 12, wherein each branch comprises a programming switch.

14. (Previously Presented) The monotonic counter of claim 12, wherein said programming resistors are two polysilicon resistors identical in size and in possible doping.

15. (Previously Presented) The monotonic counter of claim 9, wherein each counting cell comprises a programming transistor in series with a programming resistor.

16. (Previously Presented) The monotonic counter of claim 9, further comprising a circuit for controlling the programming of each of the counting cells, capable of providing individual control signals to the programming switches.

17. (Previously Presented) The monotonic counter of claim 9, wherein the decreasing includes irreversibly decreasing the value of the polysilicon resistor.